REMARKS

Claims 1-14 are now pending in this application for which applicants seek reconsideration.

Amendment

Applicants propose amending Figs. 13, 14a, 14b, and 21-24(b) of the formal drawings filed June 8, 2001 to remove the informalities noted by the examiner. Non-elected claims 15-28 have been canceled. Claim 2 has been amended to remove the informality identified by the examiner, namely changing "second" to --offset– to obviate the §112, 1st ¶ rejection. Claims 1 and 4 have been amended to positively recite that the offset region becomes a depletion layer when the device is turned OFF, as was argued in the last reply. See the paragraph spanning pages 26-27 of the present disclosure for support. As this aspect of the invention was previously presented, applicants submit that the present Amendment does not present any new issue. No new matter has been introduced.

Art Rejection

The examiner rejected claims 1-12 less than 35 U.S.C.§ 102(b) as anticipated by Kitamura (USP 5,705,842), and rejected claims 13 and 14 less than 35 U.S.C. § 103(a) as unpatentable over Kitamura. Applicants traverse these rejections because Kitamura would not have taught the claimed offset region, which becomes a depletion layer when the device is turned OFF.

Independent claims 1 and 4 each call for an offset region comprising a plurality of sub-regions aligned between the second region and the third region. As claimed, the impurity concentrations of the sub-regions are different from each other. When the device is OFF, the offset region becomes a depletion layer, which is useful for raising the breakdown voltage.

The examiner continues to argue that Kitamura's regions 3, 31 correspond to the claimed offset region. As explained in the last reply, Kitamura's regions 3, 31 cannot correspond to the claimed offset regions because they cannot sever as a depletion layer when the device is OFF. Indeed, if Kitamura's subregions 3, 31, which the examiner alleges to correspond to the claimed

offset region, is made to serve as a depletion layer when its device is turned OFF, a punch through effect will flow current between its electrodes 11 and 12. That will make the device inoperable because the device cannot be turned OFF, resulting in an uncontrollable device. Therefore, one of ordinary skill in the art would have readily understood that Kitamura's subregions could not be made to serve as a depletion layer. Indeed, Kitamura specifically would have taught away from making its subregions 3, 31 serve as a depleting layer when the device is turned OFF since its subregions 3, 31 must be used to prevent its n^+ drain region 8 from conducting to the source electrode 11 (which is in contact with the subregions 3, 31) when the device is turned OFF. Moreover, to prevent the turn-ON of a parasitic NPN transistor (8-2-3 or 8-2-31), it is necessary for the subregions 3, 31 to have a high impurity concentration. See the last line of column 1, where it describes that the subregions have deep p^+ regions 3, 31. This further proves that Kitamura's subregions 3, 31 cannot be serve as a depletion layer. Applicants submit that Kitamura's subregions at best can be construed to correspond to the claimed second region, but cannot be construed to correspond to the claimed offset region.

Conclusion

Applicants submit that claims 1-14 patentably distinguish over the applied reference and thus urge the examiner to issue an early Notice of Allowance. Should the examiner have any issues concerning this reply or any other outstanding issues remaining in this application, applicants urge the examiner to contact the undersigned to expedite prosecution.

Respectfully submitted,

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ATTACHMENT

MARKED UP VERSION

IN THE CLAIMS:

Claims 1, 2, and 4 have been amended as follows:

--1. (Twice Amended) A semiconductor device exhibiting a high breakdown voltage, the semiconductor device comprising:

a first region of a first conductivity type;

a second region of a second conductivity type formed selectively in the surface portion of the first region;

a third region of the first conductivity type formed selectively in the surface portion of the first region, the second region and the third region being spaced apart from each other;

a fourth region of the first conductivity type formed selectively in the surface portion of the second region;

an offset region of the second conductivity type formed selectively in the surface portion of the first region between the second region and the third region;

a first insulation film on the offset region;

a gate electrode above the extended portion of the second region extending between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region; and

a second main electrode on the third region;

wherein the offset region comprises a plurality of sub-regions aligned between the second region and the third region, the impurity concentrations of the sub-regions being different from each other, and.

wherein the offset region becomes a depletion layer when the device is turned OFF.--

--2. (Twice Amended) The semiconductor device according to Claim 1, wherein the depths of the sub-regions of the [second]offset region are different from each other.--

--4. (Twice Amended) A semiconductor device exhibiting a high breakdown voltage, the semiconductor device comprising:

a semiconductor substrate of a second conductivity type;

a first region of a first conductivity type formed selectively in the surface portion of the semiconductor substrate;

a second region of the second conductivity type formed selectively in the surface portion of the semiconductor substrate;

a third region of the first conductivity type formed selectively in the surface portion of the first region;

the second region and the third region being spaced apart from each other;

a fourth region of the first conductivity type formed selectively in the surface portion of the second region;

an offset region of the second conductivity type formed selectively in the surface portion of the first region between the second region and the third region;

a first insulation film on the offset region;

a gate electrode above the extended portion of the second region extending between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region; and

a second main electrode on the third region;

wherein the offset region comprises a plurality of sub-regions aligned between the second region and the third region, the impurity concentrations of the sub-regions being different from each other, and

wherein the offset region becomes a depletion layer when the device is turned OFF.--